Laboratory #2
MOSFET Differential Pairs

I. Objectives

1. Understand the basics of MOSFET differential pairs
2. Understand the importance of CMRR (Common-Mode Rejection Ratio) in OPAMP design

II. Components and Instruments

1. Components
   (1) MOSFET array IC : CD4007 ×1
   (2) Resistor : 10kΩ ×5, 100kΩ ×2, 1MΩ ×1
   (3) Capacitor : 0.1μF ×2
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Digital multimeter (Keysight 34450A)
   (3) Oscilloscope (Agilent MSOX 2014A)

III. Reading

1. Section 7.1-7.6 and 8.1-8.9 of “Microelectronics Circuits 6th edition, Sedra/Smith”.

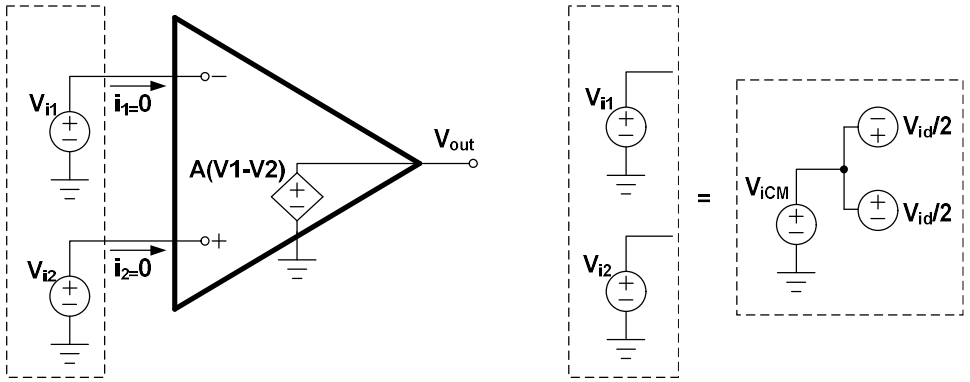
IV. Preparation

1. Introduction

   The amplifiers were introduced from characteristics of transistors to the fundamentals of single stage and multistage amplifier configurations. However, circuits are usually suffered from noises while operating in practical conditions, which result in the degradation of the signal-to-noise ratio. Hence, Lab.2 will introduce a general solution for increasing the noise immunity of an amplifier, and it is a critical issue in the design of an amplifier.

Differential-pair or differential-configuration is a widely used building block in analog integrated-circuit design. The input signal can be modeled as a differential

signal superposing on a common- mode signal as shown in Fig. 2.1 (b). The differential gain (A_d) is defined as the output voltage (V_{out} in Fig. 2.1 (a)) divided by the differential input voltage (V_{i1} and V_{i2} in Fig.2.1 (b)). Other than that, the common-mode gain (A_{CM}) is defined as the output voltage (V_{out} in Fig. 2.1 (a)) divided by the common-mode input voltage (V_{iCM} in Fig. 2.1 (b)). Differential gain represents the ideal signal gain without noise perturbations. Common-mode gain denotes the contribution of common-mode noise to the output voltage.



(a) Equivalent circuit of an ideal amplifier (b) Equivalent input signal model

Fig. 2.1 Ideal amplifier model

There is a performance index showing the noise immunity of an amplifier, which is called “Common-Mode Rejection Ratio, CMRR”. CMRR is defined as the differential gain divided by common-mode gain, which is shown as Eq. (1).

$$CMRR = \frac{A_d}{A_{CM}} \qquad (1)$$

From the equation, CMRR can be increased with larger differential gain and smaller common-mode gain. Or, in other words, the common-mode gain should be reduced in circuit design to prevent the signal from being perturbed by the common-mode noise.

2. MOSFET differential amplifier

Lab.2 introduces the CMOS differential amplifier as shown in Fig. 2.2, where Fig. 2.2 (a) and (b) shows the measurement of differential and common-mode gain respectively.

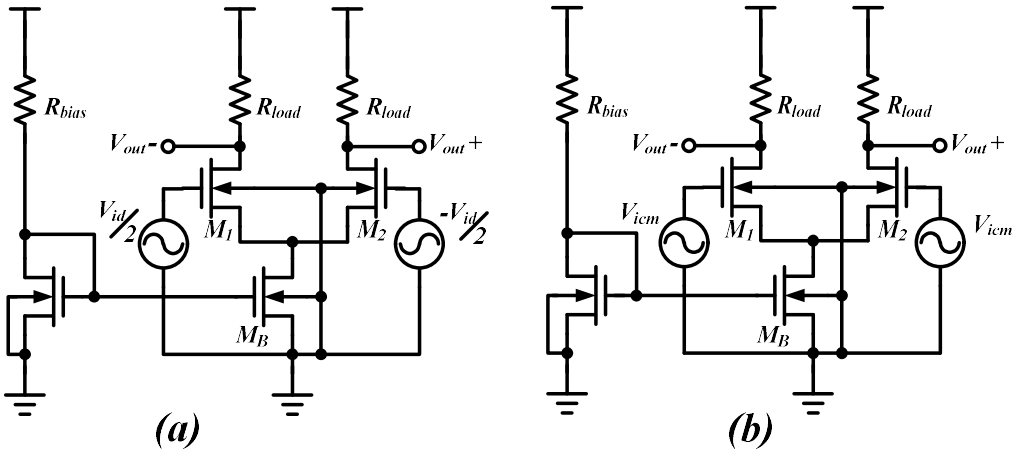


Fig. 2.2 Differential amplifier with the measurement of
(a) differential gain (b) common-mode gain

According to the topology shown in Fig. 2.2, the differential gain can be represented as Eq. (2). The differential amplifier can be considered as the superposition of a CS-CG amplifier (M1-M2) and CS amplifier (M2), thus the order of the DC gain can be estimated as $g_m r_o$.

$$A_d = g_m\left(R_{load} // r_{o2}\right) \quad r_o \text{ is the output resistance of MOSFET} \qquad (2)$$

The analysis of common-mode gain can be started from Fig. 2.3.

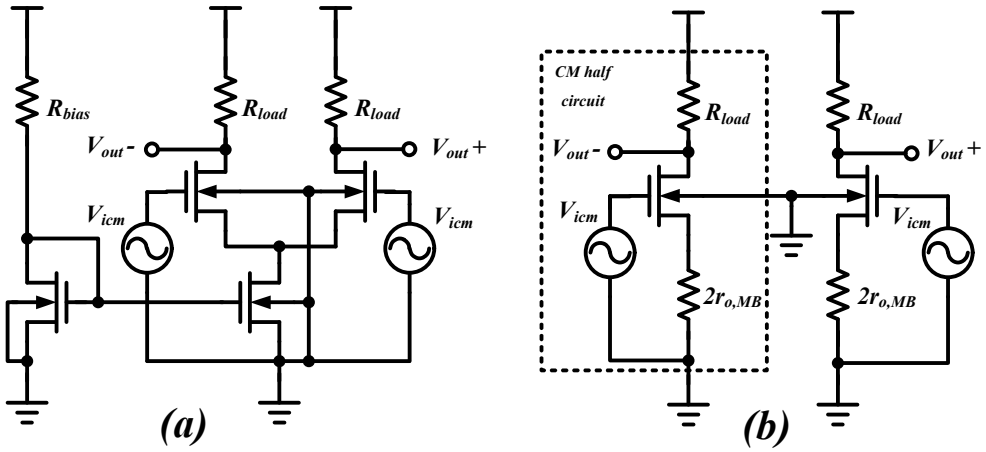


Fig. 2.3 Differential amplifier with the measurement of
(a) common-mode gain (b) half-circuit common-mode gain

The half circuit for analyzing the common-mode gain is shown in Fig. 2.3(b), assume that the transconductance of all MOSFETs are all equal to g_m and the half-circuit common-mode gain can be expressed as Eq. (3).

$$A_{cm} = \frac{-R_{load}}{1/g_m + 2r_O} \qquad (3)$$

Therefore, CMRR could be derived and simplified as shown in Eq. (4). Detailed explanations can be found in reading 1.

$$CMRR = \left| \frac{A_d}{A_{cm}} \right| = g_m r_O \qquad (4)$$

It should be noted that, in Eq. (4), the mismatches of load resistance and devices are not considered. For discrete components, the mismatches are even worse. Thus differential pair is widely implemented on-chip, which can greatly reduce the mismatches and can be further reduced with experienced layout techniques.

The frequency response of the common-mode gain can be derived with the mismatches of the components in the CMOS differential amplifier. As the load resistance mismatch is considered, the frequency response of the common-mode gain can be derived as Eq.(5), where R_{SS} and C_{SS} is the resistance and capacitance seen into the drain node of current source M_B in Fig. 2.3.

$$A_{cm} = \frac{-R_D}{2R_{SS}} \left(\frac{\Delta R_D}{R_D} \right) \left(1 + sC_{SS}R_{SS} \right) \qquad (5)$$

The Bode plot can be roughly expressed as Fig. 2.4.

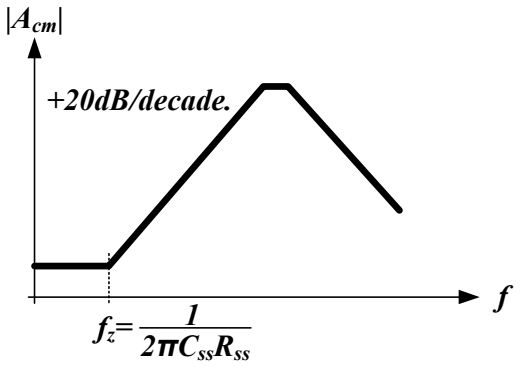


Fig. 2.4 Frequency response of the common-mode gain

V. Exploration

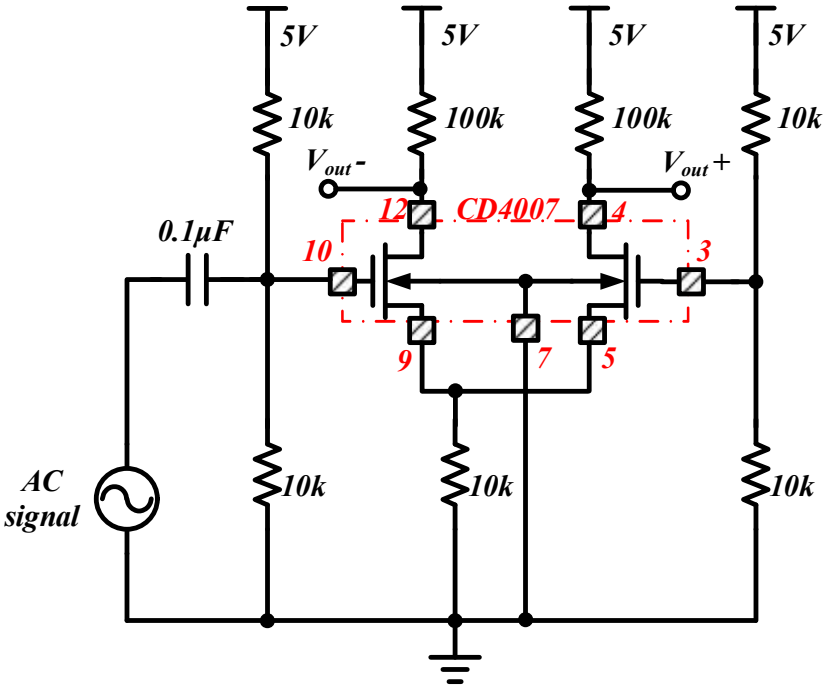


Fig. 2.5 Setup of differential gain of the CMOS differential amplifier

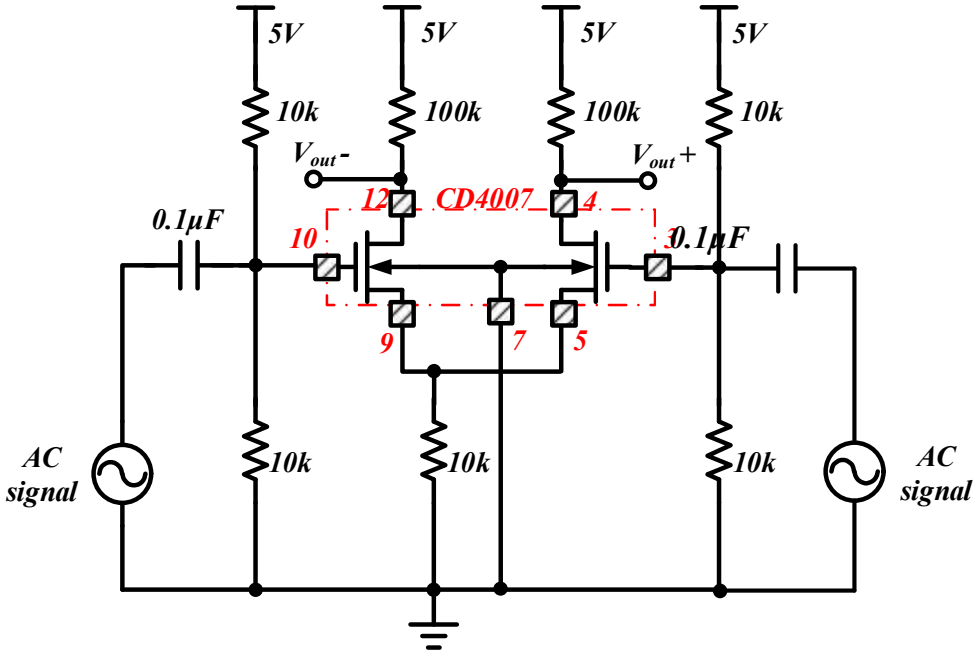


Fig. 2.6 Setup of common-mode gain of the CMOS differential amplifier

1. Explore the differential gain of the CMOS amplifier as shown in Fig. 2.5. Varies the frequency of input signal (SINE wave), record the $V_{do,p-p}$ in the Table 2.1 in the report.

Table 2.1

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{do,p-p}$ (mV)	$V_{do,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

2. Explore the common-mode gain of the CMOS differential amplifier as shown in Fig. 2.6, record the $V_{co,p-p}$ in the Table 2.2 in the report.

Table 2.2

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{co,p-p}$ (mV)	$V_{co,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

3. Calculate the CMRR of the CMOS differential amplifier

$$\left(CMRR = \frac{A_d}{A_{CM}} = Gain_{do,p-p} - Gain_{co,p-p}(dB) \right) \quad (6)$$

Fill in the corresponding values of the gain and the calculation result of CMRR in the table as shown below, which is Table 2.3 in the report.

Table 2.3

Freq. (Hz)	$Gain_{do,p-p}$ (dB)	$Gain_{co,p-p}$ (dB)	$Gain_{do,p-p}$-$Gain_{co,p-p}$ (dB)
20			
100			
1k			
10k			
20k			
30k			
40k			
50k			
100k			
200k			
500k			
700k			
1Meg			

4. To understand how the mismatch problem affects the CMRR performance, add an additional 1MΩ resistor to one of the outputs, which increases the loading resistor mismatch. Setup of the differential gain and common-mode gain are shown in Fig. 2.7 and Fig. 2.8, respectively. Measure the differential gain and common-mode gain, then calculate its CMRR. Fill in the differential output voltage and gain in Table 2.5. the common-mode output voltage and gain should be filled in Table 2.6, while the differential gain, common-mode gain and CMRR should be filled in Table 2.7

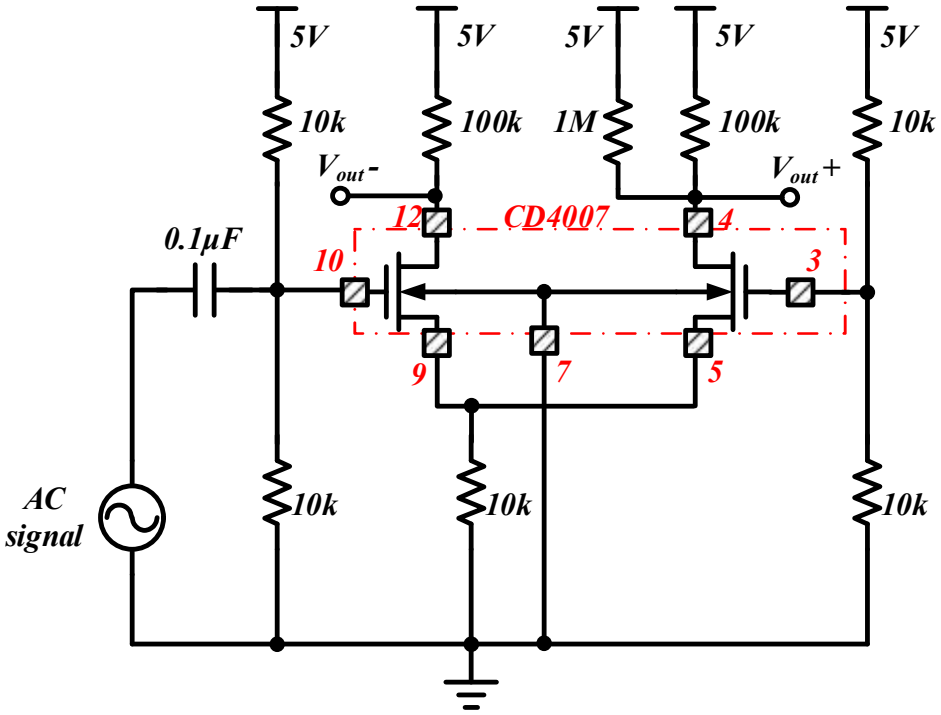


Fig. 2.7 Setup of differential gain of the CMOS differential amplifier with extra loading mismatch

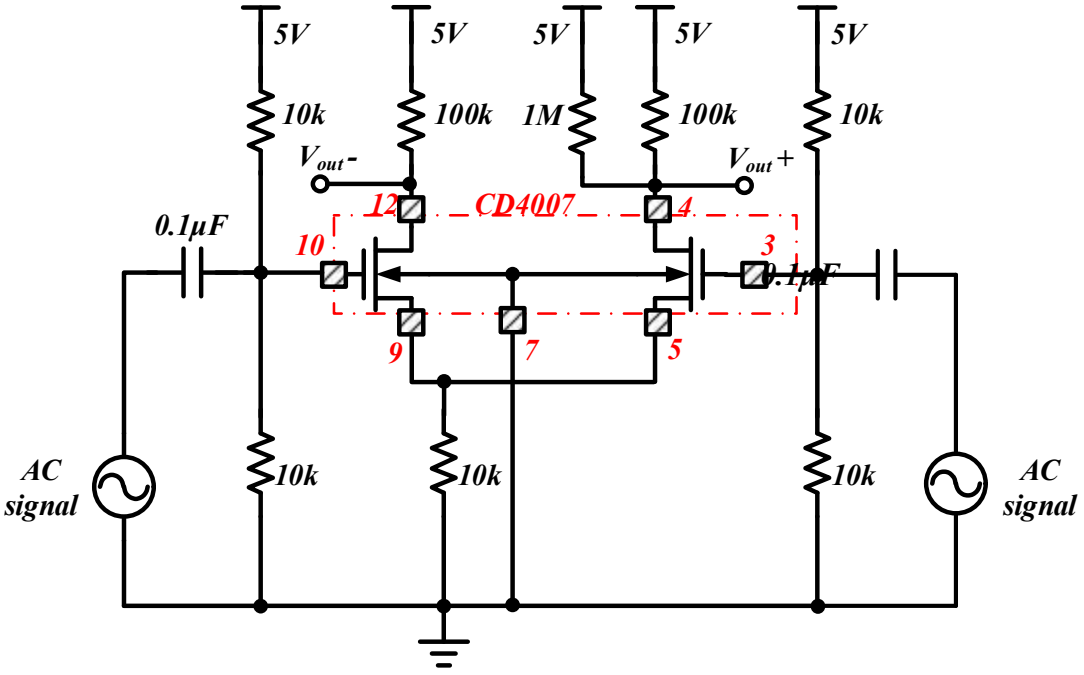


Fig. 2.8 Setup of common-mode gain of the CMOS differential amplifier with extra loading mismatch

Laboratory #2 Pre-lab

Class:

Name: Student ID:

1. Explore the CMRR of CMOS differential amplifier

   (1) Use PSpice to do the AC analysis on the circuit in Fig. 2.9. Show the plot of frequency response of V_{do}/Vi (dB) and explain the result. Note that the frequency range is set from 100 Hz to 10 GHz, and resolution is set as 10 points per decade

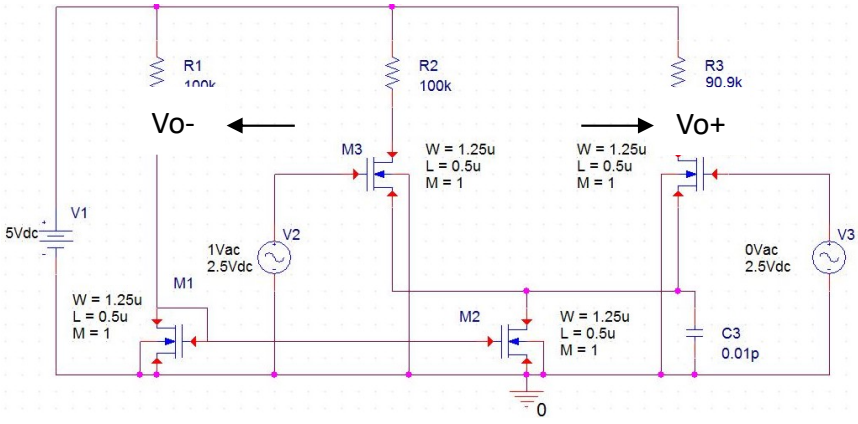


Fig. 2.9 Differential amplifier with differential input

Table 2.4 Values of components' parameters of differential MOSFET amplifier

Component	Spec.	
	W/L (μm)	M
M1	1.25/0.5	1
M2	1.25/0.5	1
M3	1.25/0.5	1
M4	1.25/0.5	1
R1	100kΩ	
R2	100kΩ	
R3	90.9kΩ (9.1kΩ mismatched value)	
C3	0.01pF	
V1	DC 5V	
V2	DC 2.5V AC1V	
V3	DC 2.5V AC0V	

(2) Change the voltage source V3 into AC 1V as shown in Fig. 2.10. Use PSpice to do the ac analysis on the circuit below, and show the plot of frequency response of V_{do}/Vi (dB).

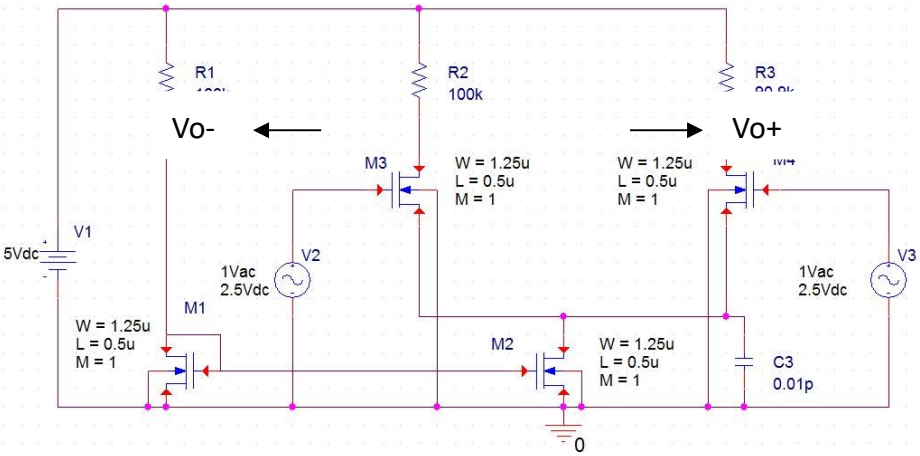


Fig. 2.10 Differential amplifier with common-mode input

(3) Calculate the CMRR at input frequency = 1 kHz, 100kHz and 10 MHz.

(4) Calculate the equivalent output resistance of M2 based on the frequency response of the common-mode gain.

(5) Calculate the corner frequency of the common-mode frequency response if the C3 is changed to 0.1pF. Then verify the calculation result using PSpice.

Laboratory #2 Report

Class:

Name: Student ID:

1. Exploration 1

(1) Differential Gain

Table 2.1

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{do,p-p}$ (mV)	$V_{do,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

(2) Common-mode Gain

Table 2.2

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{co,p-p}$ (mV)	$V_{co,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

(3) CMRR Calculation $\left(CMRR = \frac{A_d}{A_{CM}} = Gain_{do,p-p} - Gain_{co,p-p}(dB) \right)$

Table 2.3

Freq. (Hz)	$Gain_{do,p-p}$ (dB)	$Gain_{co,p-p}$ (dB)	$Gain_{do,p-p}$-$Gain_{co,p-p}$ (dB)
20			
100			
1k			
10k			
20k			
30k			
40k			
50k			
100k			
200k			
500k			
700k			
1Meg			

(4) Differential Gain with Extra Resistor Mismatch

Table 2.4

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{do,p-p}$ (mV)	$V_{do,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

(5) Common-mode Gain with Extra Resistor Mismatch

Table 2.5

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{co,p-p}$ (mV)	$V_{co,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
1k	200		
10k	200		
20k	200		
30k	200		
40k	200		
50k	200		
100k	200		
200k	200		
500k	200		
700k	200		
1Meg	200		

(6) CMRR Calculation with Extra Resistor Mismatch

$$\left(CMRR = \frac{A_d}{A_{CM}} = Gain_{do,p-p} - Gain_{co,p-p}(dB) \right)$$

Table 2.6

Freq. (Hz)	$Gain_{do,p-p}$ (dB)	$Gain_{co,p-p}$ (dB)	$Gain_{do,p-p}$-$Gain_{co,p-p}$ (dB)
20			
100			
1k			
10k			
20k			
30k			
40k			
50k			
100k			
200k			
500k			
700k			
1Meg			

2. Problem 1

There is another important issue about the design of differential pair, which is the offset problem. The MOSFET differential pair in Fig.2.9(a) is suffered from the deviation of load resistance $\triangle R_D$, and the process deviation $\triangle$(W/L), which is then resulted in $V_{OS}=f(\triangle R_D, \triangle(W/L))$. Other than that, Fig. 2.9(b), BJT differential pair is suffered from the similar problems, which are $\triangle R_C$ and $\triangle I_S$. Explain that which configuration has better offset immunity. (Hint: in general, taking V_{OV} as 100mV in MOSFET differential pair)

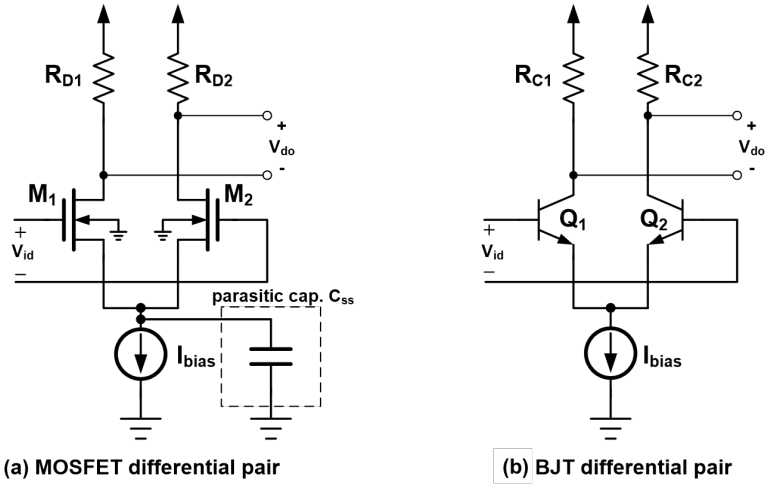


Fig. 2.11 (a) MOSFET (b) BJT differential pair

3. Problem 2

Use MATLAB or Excel to plot common-mode gain, differential gain and CMRR using measurement and calculation results respectively. Compare the differences between the differential amplifier with and without extra resistor mismatch. Also, list other possible mismatch sources during circuit design. (e.g. Resistor mismatch)

4. Bonus

Derive the transfer function of the common-mode gain of Fig. 2.3 (a), and explain how common-mode gain affects the performance of CMRR.

5. Conclusion